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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/613,695	07/10/2000	Byung-in Ma	1293.1125/MDS	9690

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EXAMINER	
AGUSTIN, PETER VINCENT	

ART UNIT	PAPER NUMBER
2652	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/613,695	MA ET AL.	
	Examiner	Art Unit	
	Peter Vincent Agustin	2652	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 17 & 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Kusano (JP 10-302277) (see translation).

In regard to claim 17, Kusano discloses an apparatus (see Drawings 1, 13 & 14) for providing a tracking error signal for an optical disk recording track, comprising: a plurality of optical detectors (Drawing 13, element 21) each of which generates an electrical signal, a matrix circuit (22) which selects and adds said electrical signals in pairs to output at least one matrixed signal, each said pair corresponding to optical information detected along a line diagonal to said recording track; a circuit (24) which binarizes each matrixed signal; a phase lock loop circuit (Drawing 13, element 127; Drawing 14, elements 161 & 163) receiving a first clock signal (PLCK, V_{plck}) and each matrixed signal, the phase lock loop circuit outputting second and third clock signals synchronized with the respective matrixed signals; and a phase detector (Drawing 13, elements 127 & 27; Drawing 14, elements 151-154) which compares a phase of the second synchronized clock signals with a phase of the third synchronized clock signals to generate the tracking error signal, wherein the tracking error signal is independent of a length of pits and/or marks on the optical disk recording track (inherent: see note). Note: the applicant's specification (see page 8, lines 19-23) discloses that "When a channel clock is used as CLK, the phase

difference Δt can be detected once every channel clock cycle T regardless of the lengths of pits or mark recorded on an optical disk". Therefore, the claimed "tracking error signal is independent of a length of pits and/or marks" would be the inherent result of the specifics, i.e., using PLL clocks, of claim 17.

In regard to claim 18, Kusano discloses first and second equalizers (Drawing 14, element 23) which increase a high frequency component of respective ones of the matrixed signals prior to respectively binarizing said matrixed signals.

Response to Arguments

3. Applicant's arguments filed March 10, 2005 have been fully considered but they are not persuasive.

a. The Applicant argues on page 3, paragraph 6 that "as described in the machine translation at paragraph 0066 "the signal PLCK of the PLL circuit 7 (refer to drawing 1) pass to the FV converter 163," clearly indicates that element 127 is not the PLL circuit". The Examiner disagrees. Kusano's description of element 7 of Drawing 1 being a PLL circuit is not a valid proof that element 127 is not a PLL circuit.

Claim 17 recites "a phase lock loop circuit receiving a first clock signal and each matrixed signal, the phase lock loop circuit outputting second and third clock signals synchronized with the respective matrixed signals". Kusano clearly shows in Drawing 13 that element 127 receives a first clock signal (PLCK) and each matrixed signal (a4 & b4) and outputs second and third clock signals (a5 & b5) synchronized with the respective matrixed signals. Therefore, the Examiner maintains that element 127 corresponds to the claimed phase lock loop circuit.

b. The Applicant states on page 3, paragraph 6 that "claim 17 of the present invention recites that the PLL circuit *receives* the first clock signal not *produces* a first clock signal (PLCK) as the reference discloses". The Examiner disagrees. The reference shows in Drawing 13 that element 127, which is read to correspond to the claimed PLL circuit, receives the first clock signal (PLCK); it does not "produce" it as argued by the Applicant.

c. The Applicant states on page 3, paragraph 8 that "the '277 reference does not disclose that the PLL circuit 7 receives any of the matrixed signals as recited in claim 17". However, as noted above, the Examiner reads element 127 as corresponding to the claimed PLL circuit.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peter Vincent Agustin whose telephone number is 571-272-7567. The examiner can normally be reached on Monday-Friday 9:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoa Thi Nguyen can be reached on 571-272-7579. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Peter Vincent Agustin
Art Unit 2652

BRIAN E. MILLER
PRIMARY EXAMINER